REMARKS

Claims 1-19 are pending in the present application, were examined, and stand rejected. In response to the Office Action, Claims 1 and 10 are amended, Claims 3, 18 and 19 are cancelled and no claims are added. Applicants respectfully request reconsideration of pending Claims 1-2 and 4-17 and withdrawal of the rejections of record in view of such amendments and the following remarks.

I. Claim Rejections Under 35 U.S.C. §102

Claims 1, 3-4, 8-10, 15, and 17-19 are rejected under 35 U.S.C. §102(e) as being taught by U.S. Patent No. 6,448,675 issued to Guenthner ("Guenthner"). Applicants respectfully traverse this rejection. Claim 1, as amended, recites:

> 1. A multi-mode processor comprising:
> a first instruction set engine to process instructions from a first instruction set architecture (ISA), the first ISA designed for a first processor having a first word size that defines the maximum number of bits that the first processor can handle as a single unit;
> a second instruction set engine to process instructions from a second ISA, the second ISA designed for a second processor having a second word size that defines the maximum number of bits that the second processor can handle as a single unit, a bit length of the second word size being greater than a bit length of the first word size;
> a mode identifier;
> a plurality of floating-point registers shared by the first instruction set engine and the second instruction set engine; and
> a floating-point unit coupled to the floating-point registers, the floating-point unit including:
> pre-processing hardware to bypass an arithmetic unit if a token exists in the input and the mode identifier indicates the second ISA mode;
> the arithmetic unit to process the input to produce an arithmetic result unless the input bypasses the arithmetic unit; and
> post-processing hardware to perform a token specific operation if a token exists in the input and bypasses the arithmetic unit to produce an output. (Emphasis added.)

Guenthner is generally directed to a data processing system that contains a processor supporting both narrow and wide instructions and narrow and wide word size fixed-point and floating-point operands, where functional units ignore extra bits of a bus wider than an

instruction width. (See Abstract.) In contrast with Claim 1, Guenthner fails to teach or suggest pre-processing hardware to bypass an arithmetic unit if a token exists in the input and the mode identifier indicates the second ISA mode, as in Claim 1. Guenthner does disclose an embodiment where 64-bit floating point registers 96 are bidirectionally coupled to and utilized by the 36-bit floating point unit 68 and the 64-bit floating point unit 98 to perform 36-bit and 64-bit floating point arithmetic functions (see col. 6, lines 24-30), however, that is something completely different from pre-processing hardware to bypass an arithmetic unit if a token exists in the input and the mode identifier indicates the second ISA mode, as in Claim 1.

Furthermore, Guenthner fails to disclose or suggest post-processing hardware to perform a token specific operation if a token exists in the input and bypasses the arithmetic unit, as in Claim 1. We submit that Guenthner is devoid of any disclosure, teaching, or suggestion regarding the use of token values within floating point registers which bypass an arithmetic unit and are provided to post-processing hardware to perform a token specific operation if a mode identifier indicates a second ISA mode, as in Claim 1.

As indicated by the Examiner, the pre-processing hardware of Claim 1 is disclosed by Guenthner in column 5, lines 46-55 and the post-processing hardware to perform a token specific operation of Claim 1 is disclosed by Guenthner in column 4, line 40 – column 5, line 22. (See pages 4 and 5, paras. A-C of the Office Action mailed 6/11/07.) However, neither these sections nor any other disclosure in Guenthner teaches or suggests pre-processing hardware to bypass an arithmetic unit if a token exists in the input and the mode identifier indicates a second ISA mode, much less post-processing hardware to perform a token specific operation if a token exists in the input and bypasses the arithmetic unit, as in Claim 1.

We submit that although the embodiment shown in FIG. 5 illustrates a processor in which 64-bit floating point unit 98 and 36-bit floating point unit 68 share the 64-bit floating point registers 96, in the embodiment shown in FIG. 6 of Guenthner the floating point registers are not shared. As shown in FIG. 6, 64-bit floating point register 96 is provided with the corresponding 64-bit floating point unit 98. Similarly, 36-bit floating point register

66 is provided to corresponding 36-bit floating point unit 68. We submit that any problems caused by the floating point systems would be avoided by implementing the embodiments disclosed by Guenthner with reference to FIG. 6, where the floating point registers are not shared. Conversely, as in Claim 1, floating point registers are shared between a first instruction set engine and a second instruction set engine, thereby requiring pre-processing hardware to bypass an arithmetic unit if a token exists in the input and a processor mode indicates a second word size ISA processor mode, as in Claim 1. At best, Guenthner is silent regarding token based post-processing hardware, as in Claim 1.

For each of the above reasons, therefore, Claim 1 and all claims which depend on Claim 1 are patentable over the cited art. Consequently, Applicants respectfully request that the Examiner reconsider and withdraw the §102(e) rejection of Claims 1, 3-4, 8 and 9.

Each of Applicants other independent claims include features similar to those highlighted in Claim 1, as discussed above. Therefore, all of Applicants other independent claims, and all claims which depend on such claims, are patentable over the cited art for similar reasons. Consequently, Applicants respectfully request that the Examiner reconsider and withdraw the §102(e) rejection of Claims 10, 15 and 17.

II. Claims Rejected Under 35 U.S.C. §103

Claims 2, 5, 7, 11, 13 and 16 are rejected under 35 U.S.C. §103(a) as being unpatentable over Guenthner and further in view of U.S. Patent Number 5,685,009 issued to Blomgren et al. ("Blomgren1") and U.S. Patent Number 5,781,750 issued to Blomgren et al. ("Blomgren2").

DEPENDENT CLAIMS

In view of the above remarks, a specific discussion of the dependent claims is considered to be unnecessary. Therefore, Applicant's silence regarding any dependent claim is not to be interpreted as agreement with, or acquiescence to, the rejection of such claim or as waiving any argument regarding that claim.

CONCLUSION

In view of the foregoing, it is submitted that Claims 1-19, as amended, patentably define the subject invention over the cited references of record, and are in condition for allowance and such action is earnestly solicited at the earliest possible date. If the Examiner believes a telephone conference would be useful in moving the case forward, he is encouraged to contact the undersigned at (310) 207-3800.

If necessary, the Commissioner is hereby authorized in this, concurrent and future replies, to charge payment or credit any overpayment to Deposit Account No. 02-2666 for any additional fees required under 37 C.F.R. §§1.16 or 1.17, particularly, extension of time fees.

Respectfully submitted,
BLAKELY, SOKOLOFF, TAYLOR, & ZAFMAN LLP

Dated: 8/10/07

By: _____
Joseph Lutz, Reg. No. 43,765

1279 Oakmead Parkway
Sunnyvale, California 94085-4040
Telephone (310) 207-3800
Facsimile (408) 720-8383

CERTIFICATE OF TRANSMISSION
I hereby certify that this correspondence is being submitted electronically via EFS Web on the date shown below to the United States Patent and Trademark Office.

_____ 8/10/07
Elaine Kwak Date